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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,306	07/01/2002	Ciaran J. Brennan	FIS920010334	6403

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EXAMINER

AUDUONG, GENE NGHIA

ART UNIT PAPER NUMBER

2818

DATE MAILED: 04/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,306	BRENNAN ET AL.	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 13-20 is/are rejected.
- 7) ☒ Claim(s) 6-12 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>2</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

1. This office acknowledges receipt of the following items from the applicant:
 - Information Disclosure Statement (IDS), filed on July 1, 2002.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Holst (U.S. Pat. No. 6,188,596).

Regarding claim 1, Holst disclose a semiconductor memory device comprising: a global data line (figure 2, global bit-line pairs 152); a plurality of primary sense amps connected to the global data line and also connected to bitlines (figure 2, primary sense amps 151 connected to the global bit-line pair 152 and also to the local bit-lines; col. 5, lines 8+), each of which is coupled to an array of memory storage cells (figure 3, memory cells 301) which are selected for write and read operations by a plurality of wordlines (figure 2); a single secondary sense amp (secondary sense amp 130) connected to the global data line, wherein the secondary sense amp receives data from the primary sense amps over the global data line, and includes a restore /writeback circuit (write circuit) to writeback data over the global data line to a primary sense amp and back into the memory (figure 2, col. 6, lines 5+ and its related description).

Regarding claim 2, Holst discloses the circuit comprising all of the limitation as of claim 1, wherein the secondary sense amp includes a latch (figure 5).

Regarding claim 3, Holst discloses the circuit comprising all of the limitation as of claim 1, wherein each primary sense amp includes at least one direct sense device, and only the gate of each direct sense device is connected to a bitline, such that the direct sense device does not provide any feedback to or alter the signal on the bitline (figure 4).

Regarding claims 4-5, Holst discloses the circuit comprising all of the limitation as of claim 1, wherein each primary sense amp includes: a pair of precharge/equalize devices, coupled between a power supply and a pair of bitlines; a pair of write switch devices, coupled between the global data line and the pair of respective bitlines; a pair of read devices, coupled between the pair of respective bitlines and the global data line; a pair of read enable switch devices, coupled in series with the pair of respective read devices and ground (figures 2, 4).

Regarding claim 13, Holst discloses the circuit comprising all of the limitation as of claim 1, wherein during a 2-cycle memory read and refresh operation, in a first memory read cycle data is transferred from one array in the memory through a primary sense amp to the secondary sense amp which is multiplexed and shared between the plurality of primary sense amps, and in a second memory refresh cycle data is transferred from the secondary sense amp to a selected primary sense amp back to the one array in the memory (col. 6, lines 5+).

Regarding claim 14, Holst discloses the circuit comprising all of the limitation as of claim 13, wherein during the 2 cycle memory write refresh operation, the wordline remains active for 2-cycles with no interim reset (col. 6, lines 5+).

Regarding claim 15, Holst discloses the circuit comprising all of the limitation as of claim 14, wherein in the first cycle a primary sense amp senses the data on a bitline, and transfers the data over the global data line as an analog level signal to a latch in the multiplexed secondary sense amp which digitizes the data, and in the second cycle the digitized data is returned over the global data line as a full-rail digital signal back to the primary sense amp which writes the data back into the memory array (col. 5, lines 55+).

Regarding claim 16, Holst discloses the circuit comprising all of the limitation as of claim 1, wherein in the first cycle a primary sense amp senses the data on a bitline, and transfers the data over the global data line as an analog level signal to a latch in the multiplexed secondary sense amp which digitizes the data, and in the second cycle the digitized data is returned over the global data line as a full-rail digital signal back to the primary sense amp which writes the data back into the memory array (col. 5, lines 55+).

Regarding claims 17 and 19, Holst discloses a primary sense amp comprising: a precharge/equalize device, coupled between a power supply and a bitline; a write device, coupled between the global data line, and the bitline; a read device, coupled between the bitline and the global data line; a read enable/switch device, coupled in series with the read device and ground; an inverter coupled between the global data line and the write device, such that inverted digitized data on the global data line is inverted and directed through the write device (see figures 2, 4).

Regarding claim 18 and 20, Holst discloses the sense amplifier circuit comprising all of the limitation as of claim 17 and 19, respectively, wherein the power supply for the inverter is switched off during a read operation, and powered on during a write operation (col. 9, lines 4+).

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Allowable Subject Matter

4. Claims 6-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not show or suggest, in addition to other element in the claim, claiming the specific structure arrangement as claimed in claims 6-12. The secondary sense amplifier of independent claim 1 and its specific components and their interconnection as claimed in claims 6-12.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (703) 305-1343.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GA
April 18, 2003



Gene N Auduong
Examiner
Art Unit 2818